TX8C1010 Datasheet

泰芯半导体
TaiXin Semiconductor

珠海泰芯半导体有限公司
Zhuhai Taixin Semiconductor Co., Limited
珠海市高新区港湾一号科创园港 11 栋 3 楼

Reversion History

Date	Version	Descriptions	Reviser
2023/09/01	V1.4	Update logo and company English name,modify ADC description.	FWF
2022/06/24	V1.3	Add IO Driving Ability Electrical Characteristics.	ZJ、HLW
2022/02/24	V1.2	Modify TX8C1010SO14B pin 8 P14 name error.	ZJ、HLW
2021/12/17	V1.1	Add HIRC and LIRC all temperature test data.	ZJ、HLW
2021/12/08	V1.0	Create from The Chinese copy.	ZJ、HLW

Contents

1 Product Overview 1
1.1 Introduction 1
1.2 Features 1
1.3 Pin Assignment 4
1.4 Encapsulate Information 6
1.5 Package Dimensions 7
1.6 Pin Description 8
2 Electrical Parameters 12
2.1 Absolute Maximum Rating 12
2.2 DC Electrical Characteristics 13
2.3 AC Electrical Characteristics 14
2.3.1. Operating Conditions During Power-On And Power-Down 14
2.3.2. Internal Reset And Power-Control Module Features 15
2.3.3. Characteristics Of External Clock Source 15
2.3.4. Characteristics Of Internal Clock Source 16
2.4 IO Driving Ability Electrical Characteristics 17
2.5 Analog Electrical Characteristics 18
2.4.1 12bit ADC Characteristics 18
2.4.2 8bit DAC Characteristics 19
2.4.3 Comparator Characteristics 20
2.6 LogicFlash DC Electrical Characteristics 20
2.7 EMC Characteristics 21
2.6.1 ESD Electrical Characteristics 21
2.6.2 Latch-Up Electrical Characteristics 21

1 Product Overview

1.1 Introduction

TX8C1010 is an **8051 core** MCU with high performance and low power consumption, whose operating frequency is up to **32MHz**. It has **4K+256 bytes** flash memory (EEPROM support) and **512 bytes SRAM**.

Analog resources: one **12-bit 200Ksps ADC** and two multi-function **comparators**.

Timer resources: Two **16-bit** advanced timers (each advanced timer supports one pair of dead band/complementary PWM), one **16-bit** general timer (supports Capture, Count and PWM functions), two **8-bit** general timers (can be combined into a 16-bit general timer and supports Capture, Count and PWM functions) and one watchdog timer.

Standard communication interface: one **SPI** interface and two **UART** interfaces.

It supports a wide range of voltage supply. The operating voltage ranges from **2.4V to 5.5V** (supports battery application scenarios), and the operating temperature range is **-40℃~ 85℃**. A variety of power-saving working modes ensure the requirements of low-power applications, and **the lowest power consumption** mode is **3uA**.

TX8C1010 provides five packaging forms: **SOP8, MSOP10, SOP14,SOP16 and QFN16**. And according to different packaging forms, the peripheral resource configuration in the device is not the same.

Applications:

- small home appliance
- electronic cigarettes
- Bluetooth charging bin and wireless charging
- toys

1.2 Features

- **Core**
  - ultra-high speed 8051 core (1T)
  - instructions are fully compatible with the traditional 8051
  - maximum operating frequency: 32MHz

- 14 interrupt sources, supporting two-level priority hardware
- support on-line download
- support code encryption
- support no power-down program

- **Operating Voltage**
  - 2.4V to 5.5V wide voltage range power supply
- **Memory**
  - 4K+256 byte Flash, which is used to store user code and supports EEPROM (typical value of erasure times: 100,000 cycle)
  - 512 byte RAM
- **Clock**
  - internal 1~32MHz high-precision HIRC, supporting calibration (error ±1%)
  - internal 64KHz low-speed LIRC, supporting calibration (error ±1%)
  - external 32.768KHz low-speed crystal oscillator requires external capacitance
- **Reset**
  - power on reset
  - low voltage reset
  - reset pin reset
  - watchdog overflows reset
- **GPIO**
  - up to 13 GPIOs
  - all ports can input and output 5V signals
  - all support rising edge/falling edge/bilateral edge interruption
  - all support the wake-up function
  - configure two levels io drive: full drive and small drive.
  - support open-drain low output mode.
  - support independently controlled pull-up and pull-down resistance of 30KΩ
- **LVD Low Voltage Detection Reset**
  - provide 4 levels of low voltage detection voltage （1.85/2.03V、2.15/2.34V、2.43/2.63V、3.34/3.63V）
- **Digital -Peripherals**
  - one SPI high-speed serial interface that supports master and slave mode
  - two UART interfaces, up to 4Mbps data rate

- **Timer Resources**
  - two 16-bit advanced timers, and each supports one pair of complementary outputs or two independent PWM outputs (with the same cycle and independent duty cycle configuration), supports dead band insertion and event braking functions, and supports single pulse mode
  - one 16-bit general timer that supports Capture, Count, and PWM functions
  - two 8-bit general timers (can be combined into a 16-bit general timer and supports Capture, Count, and PWM functions), which supports infrared sending and receiving functions (two timers are required)
  - one watchdog timer
- **High Security**
  - support 16-bit CRC check to ensure data accuracy
- **Low Power Consumption**
  - support low-power modes of Idle, Stop and Sleep
  - static power consumption is 3uA at 25℃
  - low power consumption wake-up time is less than 100us
- **A high Precision 12-bit Analog-To-Digital Converter (ADC)**
  - the convert clock supports maximum frequency of 4MHz and maximum speed of 200Ksps
  - offset correction step is 2mV, DNL +-2 INL +-4
  - 13 external input channels and 2 analog channels
  - The effective ADC bit about 10 bits(5V voltage regulator power supply,the ADC is connected to the chip’s VCC via internal switch,this voltage is used as the reference voltage of ADC,ADC at full scale equals VCC)
- **Two Analog Comparators (ACMP)**
  - two low offset comparator, and collected step is 1mV
  - the comparators support negative input precise BG or 120 voltage dividing levels of VDDADC
  - both two comparators support rail-to-rail input mode and their positive and negative ends support two GPIOs respectively
  - support dry suction protection
  - support short circuit protection
- **High Reliability**
  - ESD HBM 6KV
  - Latch-up ±200 mA at 25℃
- **96-bit Chip Unique ID (UID)**
- **Encapsulation**

- Die Form
- SOP8 / MSOP10 / SOP14 / SOP16/QFN16

- **Operating Temperature Range**
  - -40℃ ~ 85℃

1.3 Pin Assignment

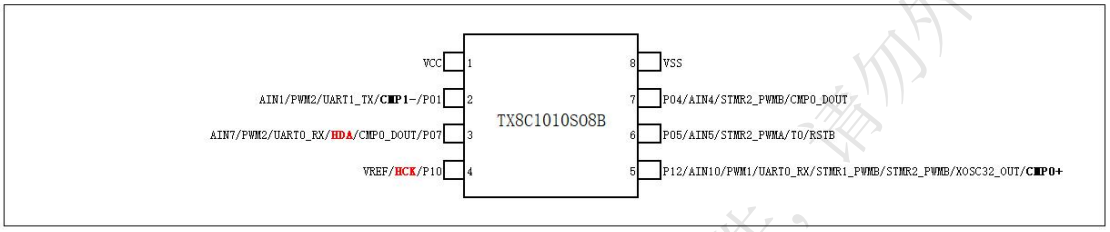


Figure 1-1 Pin of TX8C1010SO8B

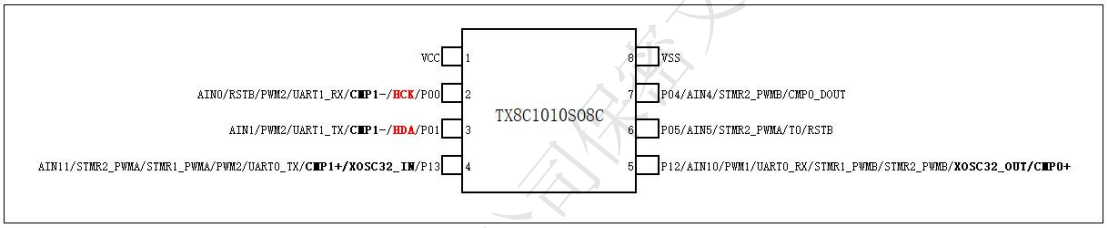


Figure 1-2 Pin of TX8C1010SO8C

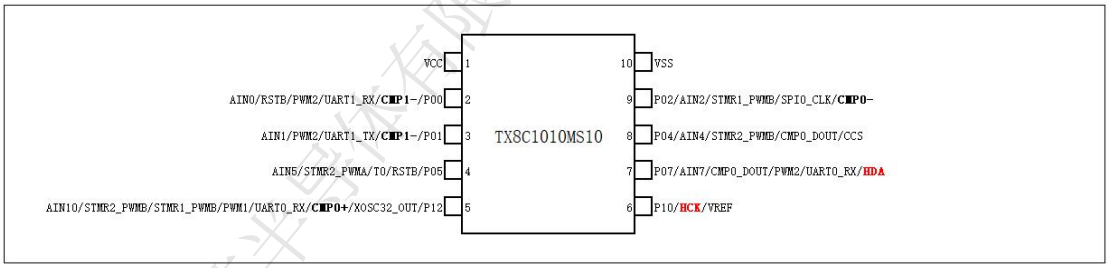


Figure 1-3 Pin of TX8C1010MS10

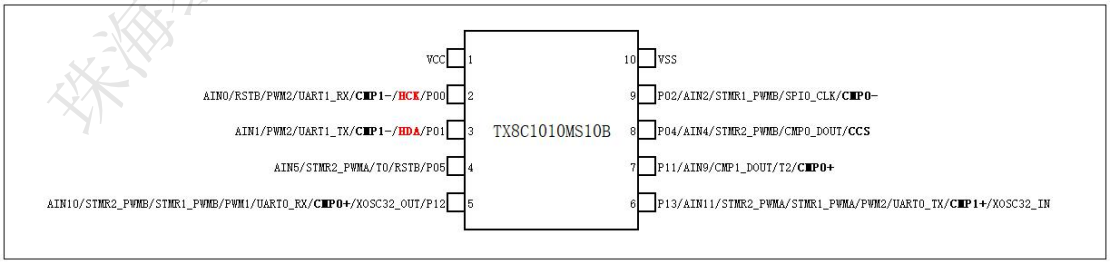


Figure 1-4 Pin of TX8C1010MS10B

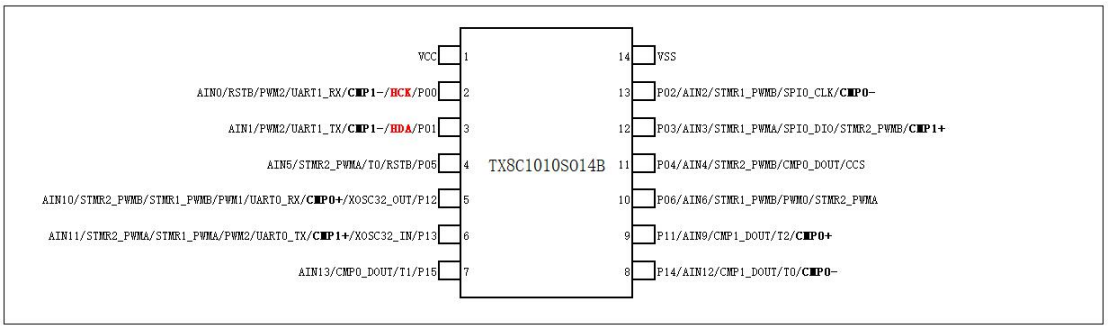


Figure 1-5 Pin of TX8C1010S014B

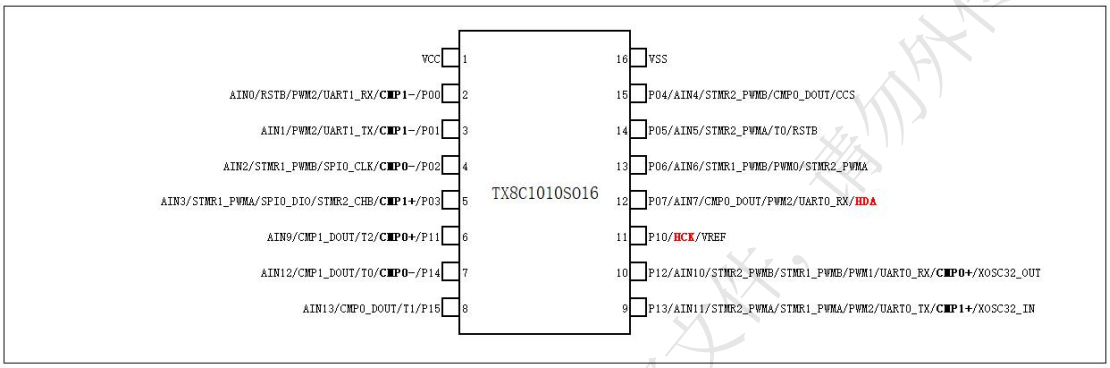


Figure 1-6 Pin of TX8C1010S016

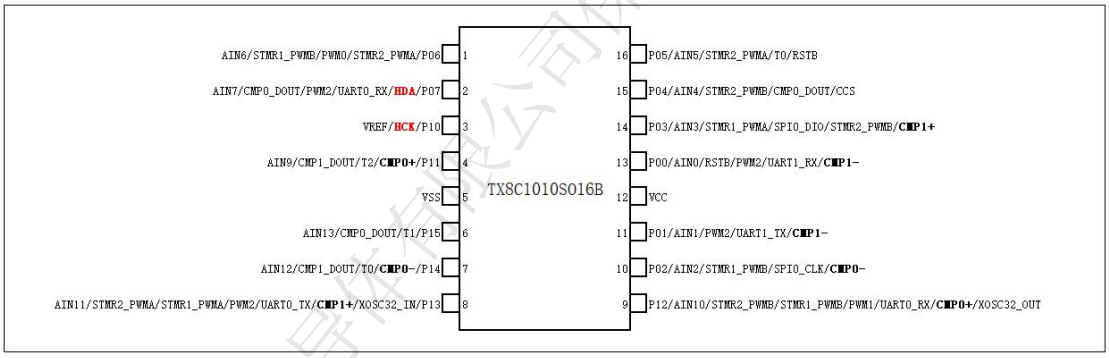


Figure 1-7 Pin of TX8C1010S016B

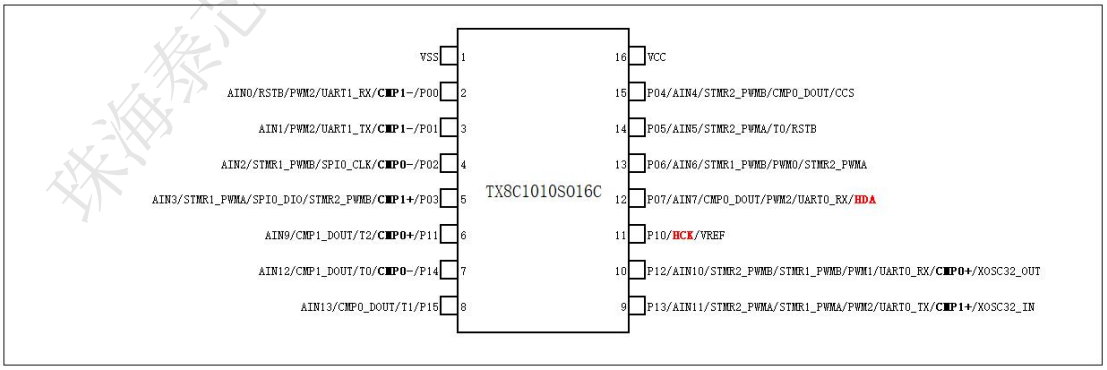


Figure 1-8 Pin of TX8C1010S016C

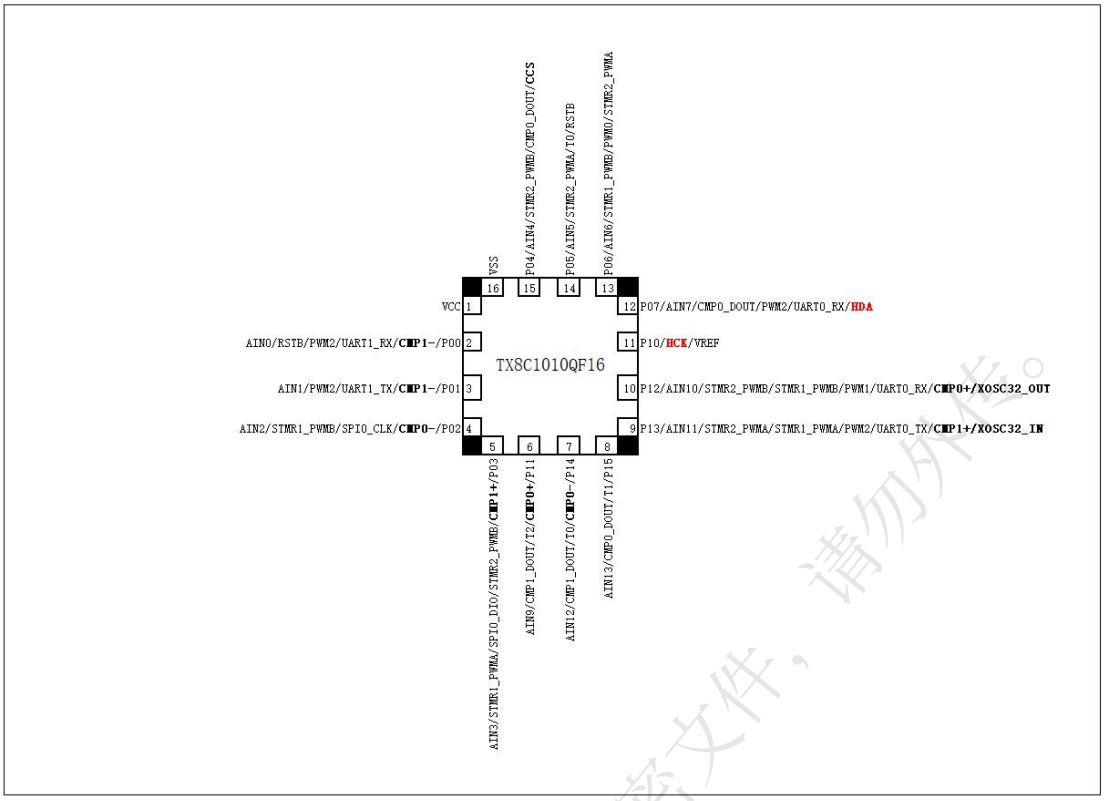


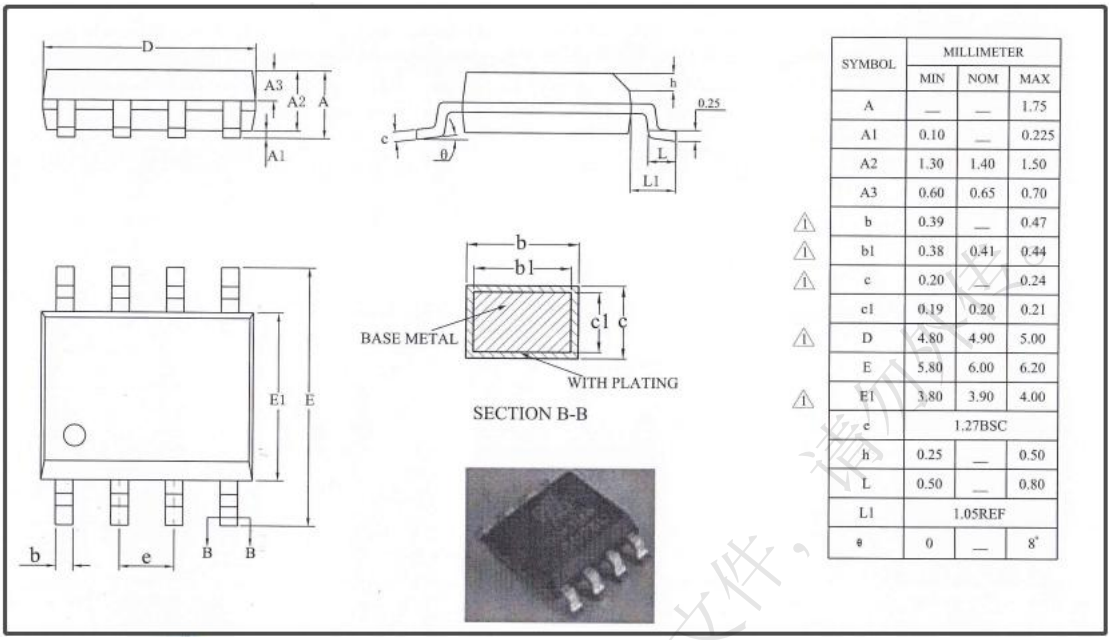
Figure 1-9 Pin of TX8C1010QF16

1.4 Encapsulate Information

The models of TX8C1010 series are shown in the following table:

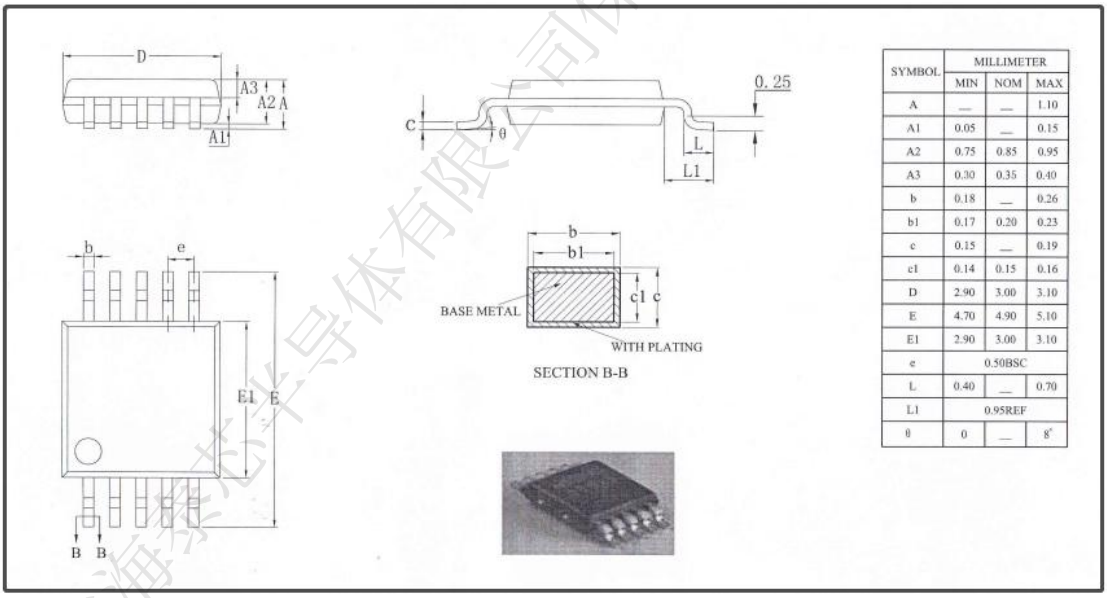
Model	Encapsulation	Packing
TX8C1010SO16	SOP16	in tube
TX8C1010SO16B	SOP16	in tube
TX8C1010SO16C	SOP16	in tube
TX8C1010SO14B	SOP14	in tube
TX8C1010MS10	MSOP10	in tube
TX8C1010MS10B	MSOP10	in tube
TX8C1010SO8B	SOP8	in tube
TX8C1010SO8C	SOP8	in tube
TX8C1010QF16	QFN16	tape reel

1.5 Package Dimensions



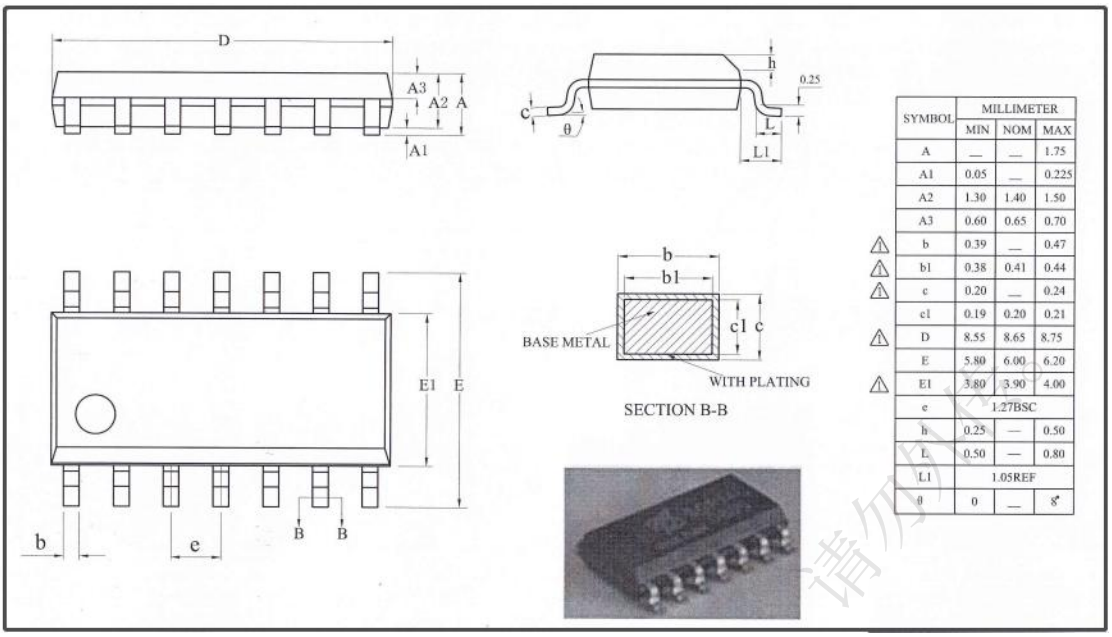
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 1-10 Encapsulation POD of SOP8



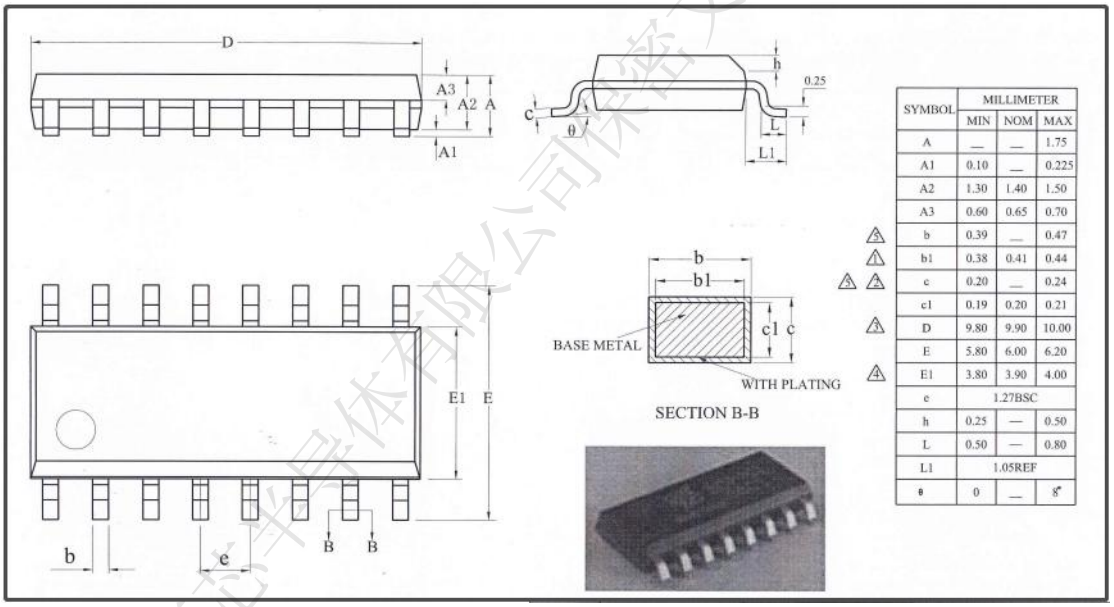
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

Figure 1-11 Encapsulation POD of MSOP10



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 1-12 Encapsulation POD of SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 1-13 Encapsulation POD of SOP16

1.6 Pin Description

Pin name	*I/O*	*Functional description*	*Reset state*	*Reuse function*
VDD	A	Power	-	nothing
GND	A	Ground	-	nothing

P00	I/O	P0 ports Each port can be set as input or output mode The input module enables internal pull-up The output module can set open-drain output	These pins default to high resistance input	**P00** **AIN0** [ADC external channel 0] **RSTB** [reset pin] **PWM2** [PWM output of Timer2] **UART1_RX** [UART1 RX receive] **HCK** [burn / debug clock pin] **CMP1-** [negative input pin of comparator 1]
P01				**P01** **AIN1** [ADC external channel 1] **PWM2** [PWM output of timer2] **UART1_TX**[UART1 TX pin] **HDA** [burn / debug data pin] **CMP1-** [negative input pin of comparator 1]
P02				**P02** **AIN2** [ADC external channel 2] **STMR1_CHB** [CHB PWM output of advanced Timer1] **SPI0_CLK** [SPI0 CLK pin] **CMP0-** [negative input pin of comparator 0]
P03				**P03** **AIN3** [ADC external channel 3] **STMR1_CHA** [CHA PWM output of advanced Timer1] **SPI0_DIO** [SPI0 DATA pin] **STMR2_CHB** [CHB PWM output of advanced Timer2] **CMP1+** [positive input pin of comparator 1]

P04				P04 AIN4 [ADC external channel 4] STMR2_CHB [CHB PWM output of advanced Timer2] CMP0_DOUT [digital output pin of comparator 0] CCS [constant current source analog pin]
P05				P05 AIN5 [ADC external channel 5] STMR2_CHA [CHA PWM output of advanced Timer2] T0 [capture input pin of general Timer0] RSTB [reset pin]
P06				P06 AIN6 [ADC external channel 6] STMR1_CHB [CHB PWM output of advanced Timer1] PWM0 [PWM output of Timer0] STMR2_CHA [CHA PWM output of advanced Timer2]
P07				P07 AIN7 [ADC external channel 7] CMP0_DOUT [digital output pin of comparator 0] PWM2 [PWM output of Timer2] UART0_RX [UART0 RX receive] HDA [burn / debug data pin]
P10	I/O	P1 ports Each port can be set as input or output mode The input module enables	P10 is pull-up on by default, and other pins default to high resistance	P10 HCK [burn / debug clock pin] VREF [ADC external reference voltage pin]

P11		internal pull-up The output module can set open-drain output	input	P11 **AIN9** [ADC external channel 9] **CMP1_DOUT** [digital output pin of comparator 1] **T2** [capture input pin of general Timer2] **CMP0+** [positive input pin of comparator 0]
P12				P12 **AIN10** [ADC external channel 10] **STMR2_CHB** [CHB PWM output of advanced Timer2] **STMR1_CHB** [CHB PWM output of advanced Timer1] **PWM1** [PWM output of Timer1] **UART0_RX** [UART0 RX receive] **CMP0+** [positive input pin of comparator 0] **XOSC32_O**[external 32.768KHz crystal oscillator output pin]
P13				P13 **AIN11** [ADC external channel 11] **STMR2_CHA** [CHA PWM output of advanced Timer2] **STMR1_CHA** [CHA PWM output of advanced Timer1] **PWM2** [PWM output of timer2] **UART0_TX**[UART0 TX transmit pin] **CMP1+** [positive input pin of comparator 1] **XOSC32_IN**[external 32.768KHz crystal oscillator input pin]

P14				P14 **AIN12** [ADC external channel 12] **CMP1_DOUT** [digital output pin of comparator 1] **T0** [capture input pin of general Timer0] **CMP0-** [negative input pin of comparator 0]
P15				P15 **AIN13** [ADC external channel 13] **CMP0_DOUT** [digital output pin of comparator 0] **T1** [capture input pin of general Timer1]

2 Electrical Parameters

2.1 Absolute Maximum Rating

Signal	Parameter	Condition	Min	Typ	Max	Unit
V_{VCC}	Operating voltage	-	2.4	5	5.5	V
V_{VCCA}	Operating voltage of analog part (ADC / DAC not used)	-	2.4	5	5.5	V
	Operating voltage of analog part (using ADC / DAC)	-	2.4	5	5.5	
$Vpin$	Pin input voltage	-	-0.3	-	5.8	V
T_A	Operating temperature	-	-40	-	105	℃
T_{ST}	Storage temperature	-	-55	-	150	℃

I_{vcc}	Total current of VCC and VCCA	-	-	-	50	mA
I_{vss}	Total current of VSS	-	-	-	50	mA

2.2 DC Electrical Characteristics

VCC - VSS = 2.4V ~ 5.5V, T_A = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCC}	Operating voltage	Fsys=0 to 32Mhz	2.4	5	5.5	V
V_{VCCA}	Operating voltage of analog part (ADC / DAC not used)	Fsys=0 to 32Mhz	2.4	5	5.5	V
	Operating voltage of analog part (using ADC / DAC)	Fsys=0 to 32Mhz	2.4	5	5.5	
I_{VDD}	Normal operating mode	VCC=5V, Fsys=32Mhz, all peripherals are turned off	-	3.73	-	mA
		VCC=5V, Fsys=16Mhz, all peripherals are turned off	-	2.90	-	mA
		VCC=5V, Fsys=8Mhz, all peripherals are turned off	-	2.485	-	mA
		VCC=3.3V, Fsys=32Mhz, all peripherals are turned off	-	3.263	-	mA
		VCC=3.3V, Fsys=16Mhz, all peripherals are turned off	-	2.491	-	mA
		VCC=3.3V, Fsys=8Mhz, all peripherals are turned off	-	2.078	-	mA
I_{sleep}	Sleep current	VDD=5V, all peripherals are turned off and IO wakes up	-	3.28	-	uA
		VDD=3.3V, all peripherals are turned off and IO wakes up	-	2.51	-	uA

V_{IL}	Low voltage input	-	VSS	-	0.3VCC	V
V_{IH}	High voltage input	-	0.5VCC	-	VCC	V
V_{hys}	I / O pin Schmitt trigger voltage hysteresis	-	-	1	-	V
R_{PU}	Equivalent pull-up resistance	-	-	26	-	kΩ
R_{PD}	Equivalent pull-down resistance	-	-	26	-	kΩ
C_{IO}	Capacitance of I / O pin	-	1.5	2	2.5	pF
V_{OL}	Low voltage output	VCC=5.0V, I_{OL}=9mA	-	-	0.5	V
		VCC=4.2V, I_{OL}=8mA	-	-	0.5	V
		VCC=3.3V, I_{OL}=6mA	-	-	0.5	V
V_{OH}	High voltage output	VCC=5.0V, I_{OL}=12mA	4	-	-	V
		VCC=4.2V, I_{OL}=6mA	3.3	-	-	V
		VCC=3.3V, I_{OL}=5mA	2.6	-	-	V

2.3 AC Electrical Characteristics

2.3.1. Operating Conditions During Power-On And Power-Down

Table 2-1 Operating conditions during power-on and power-down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VCC}	V_{VCC}	T_A = 27℃	5	-	uS
t_{VCCA}	V_{VCCA}		5	-	uS

Table 2-2 Status during power-on and power-down

Chip status	Power on			Power down	
	Power on protection	Power on reset	Normal operation	Low power reset	Power down reset
supply voltage (V)	<1.8	1.8 - 2.4	>2.4	<1.85	<1.6

System power consumption (uA)	<0.2	300	Power on normally, and the power consumption is determined by the frequency of the system clock and peripherals.	300	<0.2

2.3.2. Internal Reset And Power-Control Module Features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC_{PVD}	Level of programmable voltage detector	LVDCON0[3:2]=0x0, power-on detection threshold, TA=25℃	-	2.03	-	V
		LVDCON0[3:2]=0x0, power -down detection threshold, TA=25℃	-	1.85	-	V
		LVDCON0[3:2]=0x1, power-on detection threshold, TA=25℃	-	2.34	-	V
		LVDCON0[3:2]=0x1, power -down detection threshold, TA=25℃	-	2.15	-	V
		LVDCON0[3:2]=0x2, power-on detection threshold, TA=25℃	-	2.63	-	V
		LVDCON0[3:2]=0x2, power -down detection threshold, TA=25℃	-	2.43	-	V
		LVDCON0[3:2]=0x3, power-on detection threshold, TA=25℃	-	3.63	-	V
		LVDCON0[3:2]=0x3, power -down detection threshold, TA=25℃	-	3.34	-	V
$V_{PVDhyst}$	VCC hysteresis	-	-	-	-	mV

Note: The above data comes from the chip performance acceptance test and is not tested in production.

2.3.3. Characteristics Of External Clock Source

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{xoscm}	Frequency of user external clock			32768		Hz
V_{BIAS}	XOSCI/XOSCO bias level	-	-	770	-	mV
V_{xoh}	XOSCI input pin high level voltage	-	-	975	-	mV

V_{xol}	XOSCI input pin low level voltage	-	-	525	-	mV
$Duty_{(xoscm)}$	Duty cycle	-	42	-	58	%
I_L	XOSCI input leakage current	-	-	1.5		uA
ACC_{xoscm}	HSE accuracy	-	-	-	-	ppm
$t_{SU(xoscm)}$	Startup time	-	-	1		s

2.3.4. Characteristics Of Internal Clock Source

Table 2-3 HIRC oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCCA}	Supply voltage	-	2.2	3.3	5.5	V
f_{HRC}	frequency	TA=25℃,Test after triming	31.68	32	32.32	MHz
ACC_{HSI}	Accuracy of oscillator	-40℃至 85℃	-	-	-	%
$t_{SU(HSI)}$	Oscillator start time	-	-	60	-	us
$I_{VCCA(HSI)}$	Oscillator power consumption	Average power consumption	-	-	1.5	mA

Following shows HIRC value under all temperature and all supply voltages condition:

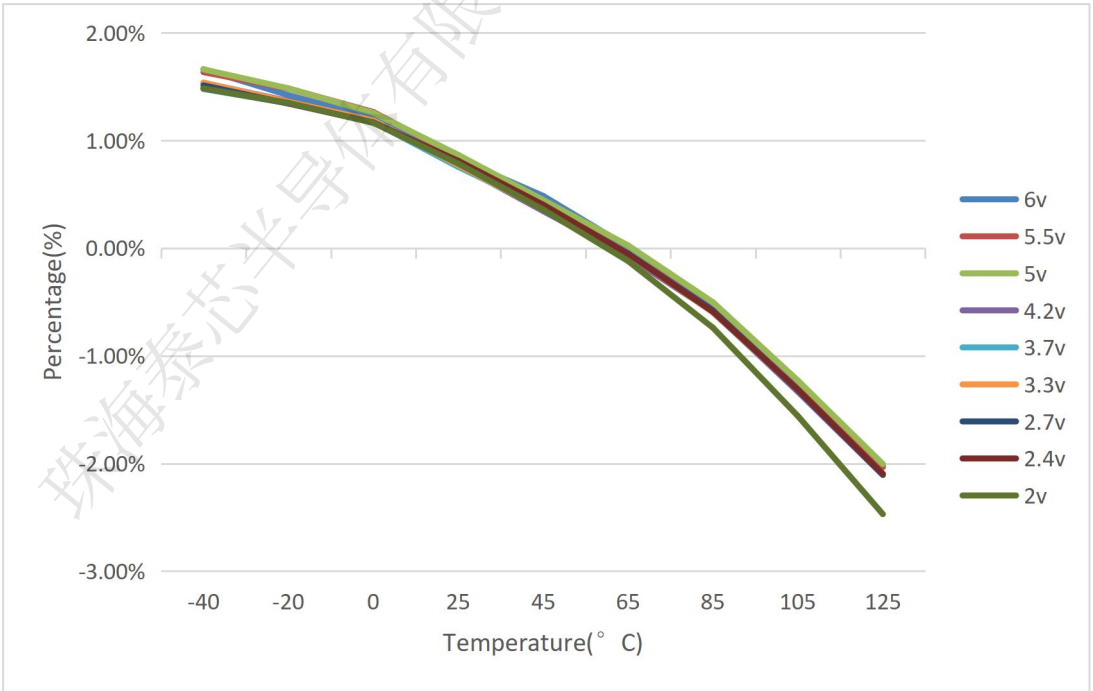


Figure 2-3 HIRC deviation under all voltage and all temperature

Table 2-4 LIRC oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LRC}	frequency	TA=25℃	-	64	-	kHz
$I_{DD(LSI)}$	Oscillator power consumption	-	-	0.5	-	uA

Following shows LIRC value under all temperature and all supply voltages condition:

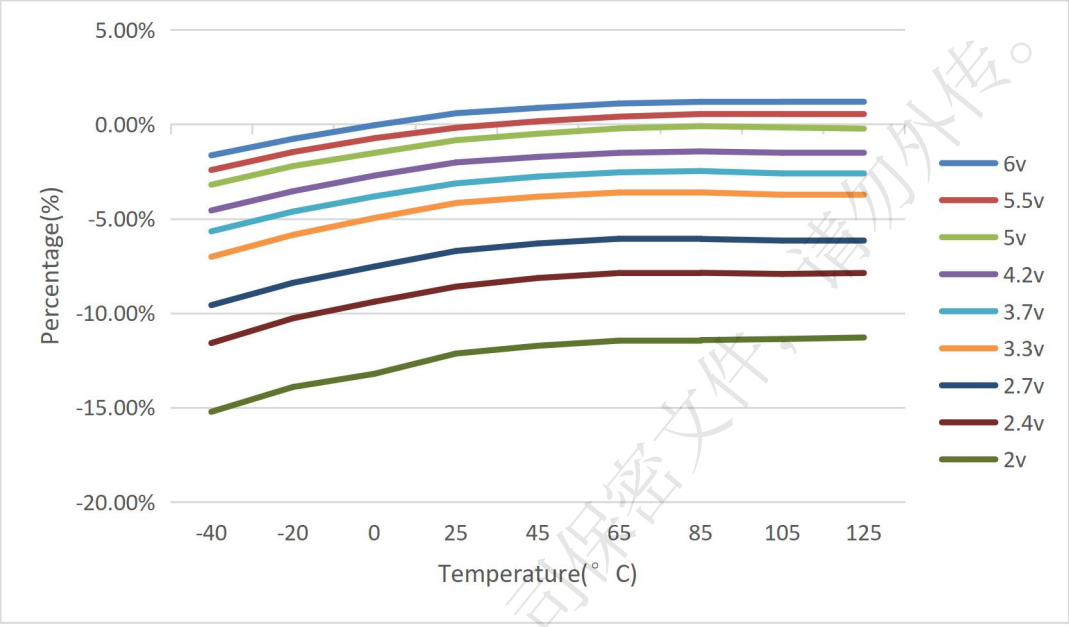


Figure 2-4 LIRC deviation under all voltage and all temperature

2.4 IO Driving Ability Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OH1}	High level output voltage Source Current	VCC=5V, IO drive level is configured as maximum, VOH=4.3V	-	25	-	mA
		VCC=5V, IO drive level is configured as maximum, VOH=0.7*VCC	-	50	-	mA
		VCC=3.3V, IO drive level is configured as maximum, VOH=0.7*VCC	-	20	-	mA
I_{OL1}	Low level output voltage Sink Current	VCC=5V, IO drive level is configured as maximum, VOL=0.5V	-	60	-	mA
		VCC=5V, IO drive level is configured as maximum, VOL=0.3*VCC	-	130	-	mA

		VCC=3.3V, IO drive level is configured as maximum, VOL=0.3V	-	30	-	mA
		VCC=3.3V, IO drive level is configured as maximum, VOL=0.3*VCC	-	70	-	mA
I_{OH0}	High level output voltage Source Current	VCC=5V, IO drive level is configured as minimum, VOH=4.3V	-	6	-	mA
		VCC=5V, IO drive level is configured as minimum, VOH=0.7*VCC	-	12	-	mA
		VCC=3.3V, IO drive level is configured as minimum, VOH=0.7*VCC	-	5	-	mA
I_{OL0}	Low level output voltage Sink Current	VCC=5V, IO drive level is configured as minimum, VOL=0.5V	-	8	-	mA
		VCC=5V, IO drive level is configured as minimum, VOL=0.3*VCC	-	17	-	mA
		VCC=3.3V, IO drive level is configured as minimum, VOL=0.3V	-	3.5	-	mA
		VCC=3.3V, IO drive level is configured as minimum, VOL=0.3*VCC	-	8	-	mA

Note: The above data is based on the test of a single io. In the application scheme, due to the limitation of the total current of 50mA, the average current of all IO cannot exceed 50mA for a long time, therwise the device life will be affected!

2.5 Analog Electrical Characteristics

2.4.1 12bit ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCCA}	Supply voltage	-	2.4	5	5.5	V
I_{VCCA}	Current consumption	-	-	480	-	uA

f_{ADC}	ADC clock frequency	-	-	-	4	MHz
Fconv	Conversion rate	-	-	-	200	KHz
V_{AIN}	Conversion voltage range	Internal 1.2V reference	0	-	1.2	V
		Internal 2.4V reference	0	-	2.4	
R_{AIN}	External input impedance	-	-	-	-	Kohm
C_{ADC}	Internal sample and hold capacitance	-	-	6.9	-	pF
t_{STAB}	Power on time	-	-	-	1100	us
t_{conv}	Sampling time	-	5		256	Tclk
Enob	-	-	-	10	-	Bit

Note: The input/output frequency of IO near the ADC input signal is not higher than 10KHz, the reference voltage of the ADC is VCC, the full scale is VCC, ENOB 10bit is the result of the test under the power supply of a 5V regulator, in practical application, the deviation of power supply will cause the loss of precision, the performance of the significant bit 10bit is not guaranteed at other voltages

2.4.2 8bit DAC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCCA}	Analog Supply voltage	-		1.2		V
I_{VCCA}	Current consumption	-	-	20	-	uA
C_L	Capacitive load	-	-	2	-	pF
R_0	Output impedance	-			60	KΩ
V_{DAC_OUT}	Voltage output	-	0.002	0.6	1.2	V
DNL	Nonlinear error	-	-	±0.5	-	LSB
INL	Linear error	-	-	2		LSB
Offset	Coding offset error 0x800	-	-	-		mV

2.4.3 Comparator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VCCA}	Analog Supply voltage	-	2.4	3.3	5.5	V
OFFSET	Offset voltage	-		2		mV
DELAY	Propagation delay	-	-	220	-	ns
I_q	Average operating current	-	-	112	-	uA

2.6 LogicFlash DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{prog}	Programming voltage	-	2.4	3.3	5.5	V
t_{prog}	Program time	1 word(2Byte)	-	160	-	us
t_{RC}	Read time	-	50	-	100	ns
t_{ERASE}	Page erase time	-	-	50	-	ms
t_{ME}	Chip erase time	-	-	50	-	ms
I_{DD}	Supply current	read	0.8	1	1.4	mA
		program	2	4	6	mA
		erase	3.3	5.3	6	mA
NEND	Endurance	Wipe and write 100,000 times in a high temperature environment of 105℃	-	100,000	-	cycle
t_{RET}	Data retention	After erasing and writing 100,000 times at room temperature, put it at 105℃ and bake at high temperature	-	10	-	year

2.7 EMC Characteristics

2.6.1 ESD Electrical Characteristics

Symbol	Ratings	Condition	Max	Unit
ESD	Electrostatic discharge (Human body mode)	TA = + 25℃, JEDEC EIA/JESD22-A114	6000	V
	Electrostatic discharge (Device Charged mode)	TA = + 25℃, JEDEC EIA/JESD22-C101-B	1000	V

2.6.2 Latch-Up Electrical Characteristics

Symbol	Parameter	Condition	Test Type	Min	Unit
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (TA = +25 ℃)	±200	mA